In the Claims:

1. (Presently Amended) An integrated circuit comprising:

a host processor interface;

a common memory bus coupled to said host processor interface;

a plurality of memory devices, each of said plurality of memory devices coupled to said common memory bus; and

a plurality of digital signal processors, each one of said plurality of digital signal processors associated with and coupled to a corresponding one of said plurality of memory devices. ~~and~~

~~a host processor interface coupled to a host processor and to said plurality of digital signal processors.~~

2. Canceled.

3. Canceled.

4. (Currently Amended) ~~The~~ An integrated circuit ~~of Claim 2 further~~ comprising:

a plurality of digital signal processors;

a host processor interface coupled to a host processor and to said plurality of digital signal processors;

a plurality of memory devices, each associated with and coupled to one of said plurality of digital signal processors and each coupled to said host processor interface;

a plurality of direct memory access devices, each associated with one of said plurality of digital signal processors and each coupled to the memory d vic associated with the respective digital signal processor; and

at least two time division multiplexing devices associate with each digital signal processor and coupled to the direct memory access device associated with each digital signal processor, each time division multiplexing device including a signal port for receiving and sending signals.

5. (Original) The integrated circuit of Claim 4 wherein:

each memory device comprises an instruction memory device and a data memory device and each direct memory access device is coupled to a data memory device.

6. (Original) The integrated circuit of Claim 5, further comprising:

a common memory bus coupling each of said instruction memory and data memory devices to said host processor interface.

7. (Original) The integrated circuit of Claim 1 further comprising an IEEE Standard 1149.1 compliant testing module connected to all digital signal processors on the integrated circuit.

8. (Original) An integrated circuit according to Claim 1 wherein:

said digital signal processors comprise ZSP400 digital signal processors.

9 Canceled.

10. Canceled.

11. (Presently Amended) ~~The~~ An integrated circuit ~~of claim 10 further~~ comprising:

at least two ZSP400 digital signal processors;

a host processor interface coupled to said at least two ZSP400 digital signal processors;

~~(a)~~ an instruction memory module and controller for and coupled to each digital signal processor;

~~(b)~~ a data memory module and controller for and coupled to each digital signal processor and to said host processor interface;

~~(c)~~ a direct memory access device for and coupled to each data memory module; and

~~(d)~~ at least two time division multiplexing devices for and coupled to each data memory module.

12. (Original) The integrated circuit of Claim 11 further comprising:

a common bus coupling each of said instruction memory modules and each of said data memory modules to said host processor interface.

13. (Presently Amended) The integrated circuit of Claim ~~9~~ 8 further comprising:

an IEEE Standard 1149.1 compliant testing module connected to all digital signal processors on the integrated circuit.

14. (Presently Amended) A method of operating at least two digital signal processors on a single integrated circuit comprising:

coupling said at least two digital signal processors to a host processor using a single host processor interface coupled to a common memory bus coupled to at least two memory devices coupled to respective ones of said at least two digital signal processors.

15. (Presently Amended) A method ~~according to Claim 14 further including:~~ of operating at least two digital signal processors on a single integrated circuit comprising:

coupling said at least two digital signal processors to a host processor using a single host processor interface;

providing an instruction memory and a data memory for each digital signal processor, and

coupling each instruction memory and data memory to its respective digital signal processor and to said host processor interface.

16. (Original) A method according to Claim 15 further including:

using a common memory bus to couple each instruction memory and each data memory to the single host processor interface.

17. ~~The~~ A method ~~of claim 14 further~~ of operating at least two digital signal processors on a single integrated circuit comprising:

coupling said at least two digital signal processors to a host processor using a single host processor interface; and

coupling said digital signal processors to multiple framers by:

(a) coupling one direct memory access device to each digital signal processor;

(b) coupling at least two time division multiplexing devices to each direct memory access device; and

(c) coupling one framer to each time division multiplexing device.

18. (Presently Amended) The method of claim 15 further comprising:

providing a direct memory access device for each data memory; and

coupling each direct memory access device to ~~a digital signal processor by coupling a data memory unit to both said direct memory access device and said digital signal processor~~ its respective data memory.

19. (Presently Amended) The method of Claim ~~11~~ 14 wherein:

each of said digital signal processors comprises a ZSP400 digital signal processor.

20. Canceled.

21. (Presently Amended) ~~The~~ A method of ~~claim 20 further~~ operating at least two ZSP400 digital signal processors on a single integrated circuit comprising:

coupling said ZSP400 digital signal processors to a host processor using a single host processor interface; and

coupling said ZSP400 digital signal processors to multiple framers by:

~~(d)~~ coupling one direct memory access device to each digital signal processor;

~~(e)~~ coupling at least two time division multiplexing devices to each direct memory access device; and

~~(a)~~ coupling one framer to each time division multiplexing device.

22. (Original) The method of claim 21 further comprising:

coupling each direct memory access device to a digital signal processor by coupling a data memory unit to both said direct memory access device and said digital signal processor.

23. (New) The integrated circuit of Claim 1, wherein each one of said plurality of memory devices are connected to said host processor interface by said common memory bus.

24. (New) The integrated circuit of Claim 1, wherein each one of said plurality of digital signal processors are connected to said common bus by said corresponding one of said plurality of memory devices.

25. (New) The integrated circuit of Claim 24, wherein each on of said plurality of memory devices are connected to said host processor interface by said common memory bus.